IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A cache memory, comprising:

a data storage ~~capable of storing~~ configured to store data which requires consistency of data with a main memory; and

a storage controller which controls ~~to store~~ storing data which does not require consistency of data with said main memory, in an arbitrary data region in said data storage, the arbitrary data region having an address space different from that of said main memory.

Claim 2 (Original): The cache memory according to claim 1, wherein said arbitrary data region is a data region designated by a programmer.

Claim 3 (Currently Amended): The cache memory according to claim 1, further comprising:

a region designating unit which specifies addresses of said arbitrary data region ~~for storing~~ configured to store data which does not require consistency of data with said main memory; and

an address coincidence determination unit which determines whether ~~or not the designated~~ a particular address coincides with the addresses designated by said region ~~designated~~ designating unit.

Claim 4 (Currently Amended): The cache memory according to claim 3, further comprising a tag unit which stores addresses of data stored in said data storage,

wherein said data storage and said tag unit ~~are composed of~~ include a plurality of ways including a plurality of indexes, respectively; and

said region ~~designated~~ designating unit specifies whether ~~or not~~ data which does not require consistency of data with said main memory is stored in [[the]] a corresponding data region unit ~~is a unit of one way~~ for each way.

Claim 5 (Currently Amended): The cache memory according to claim 4, further comprising:

a refill information storage which stores refill history information of refill in said data storage; and

a refill object selector which selects ways to be refilled based on the refill history information stored in said refill information storage and addresses designated by said region designating unit.

Claim 6 (Currently Amended): The cache memory according to claim 5, wherein said region ~~designated~~ designating unit includes:

an address setting unit provided for each way, which sets addresses of data region for storing data which does not require consistency of data with said main memory; and

a setting information storage provided for each way, which stores flag information indicative of whether ~~or not~~ a prescribed address is set to said address setting unit,

wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information.

Claim 7 (Currently Amended): The cache memory according to claim 1, wherein a look-aside type connection ~~method~~ configuration in which said main memory and said cache memory are connected to a common system bus, and a write-through writing ~~method~~

configuration in which data is written to said main memory and said cache memory at the same time are adopted.

Claim 8 (Currently Amended): A processor which adopts a look-aside type connection ~~method~~ configuration in which a main memory and a cache memory are connected to a common system bus, and a write-through writing ~~method~~ configuration in which data is written to said main memory and said cache memory at the same time, wherein said cache memory includes:

a data storage capable of storing data which requires consistency of data with said main memory; and

a storage controller which controls ~~to store~~ storing data which does not require consistency of data with said main memory, in an arbitrary data region in said data storage, the arbitrary data region having an address space different from that of said main memory.

Claim 9 (Original): The processor according to claim 8, wherein said arbitrary data region is a data region designated by a programmer.

Claim 10 (Currently Amended): The processor according to claim 8, further comprising:

a region ~~designated~~ designating unit which specifies addresses of said arbitrary data region configured to store data which does not require consistency of data with said main memory; and

an address coincidence determination unit which determines whether ~~or not the designated~~ a particular address coincides with the ~~address~~ addresses designated by said region ~~designated~~ designating unit.

Claim 11 (Currently Amended): The processor according to claim 10, further comprising a tag unit which stores addresses of data stored in said data storage,

wherein said data storage and said tag unit ~~are composed of~~ include a plurality of ways including a plurality of indexes, respectively; and

said region ~~designated~~ designating unit specifies whether ~~or not~~ data which does not require consistency of data with said main memory is stored in [[the]] a corresponding data region unit ~~is a unit of one way~~ for each way.

Claim 12 (Currently Amended): The processor according to claim 11, further comprising:

a refill information storage which stores history information of refill in said data storage; and

a refill object selector which selects ways to be refilled based on the refill history information stored in said refill information storage and addresses designated by said region designating unit.

Claim 13 (Currently Amended): The processor according to claim 12, wherein region ~~designated~~ designating unit includes:

an address setting unit provided for each way, which sets addresses of data region for storing data which does not require consistency of data with said main memory; and

a setting information storage provided for each way, which stores flag information indicative of whether ~~or not~~ a prescribed address is set to said address setting unit,

wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information.

Claim 14 (Currently Amended): A cache control method which adopts a look-aside type connection method in which a main memory and a cache memory are connected to a common system bus, and a write-through writing method in which data is written into said main memory and said cache memory at the same time, comprising

controlling ~~to store~~ storage of data which does not require consistency of data with said main memory in an arbitrary data region in a data storage ~~to store data which does not require consistency of data said main memory~~, the arbitrary data region having an address space different from that of said main memory.

Claim 15 (Original): The cache control method according to claim 14, wherein said arbitrary data region is a data region designated by a programmer.

Claim 16 (Currently Amended): The cache control method according to claim 14, further comprising:

designating, in advance, addresses of said data region to store data which does not require consistency of data with said main memory; and

determining whether ~~or not required~~ a particular address coincides with the designated address.

Claim 17 (Currently Amended): The cache control method according to claim 16, wherein said data storage and a tag unit which stores addresses of data stored in said data storage ~~are composed of~~ include a plurality of ways including a plurality of indexes; and

it is designated whether ~~or not~~ data which does not require consistency of data with said main memory is stored in [[the]] a corresponding data region unit ~~in unit of one way~~ for each way.

Claim 18 (Currently Amended): The cache control method according to claim 17, further comprising:

storing refill history information of refill in said data storage; and

selecting the way to be refilled based on the stored history information and the ~~address~~ addresses designated by said region ~~designated~~ designating unit.

Claim 19 (Currently Amended): The cache control method according to claim 18, comprising:

setting addresses of a data region to store data which does not require consistency of data with said main memory for each way;

storing the flag information indicative of whether ~~or not~~ addresses are set for each way; and

selecting the way to be refilled based on said refill history information and said flag information.